

FIG. 1

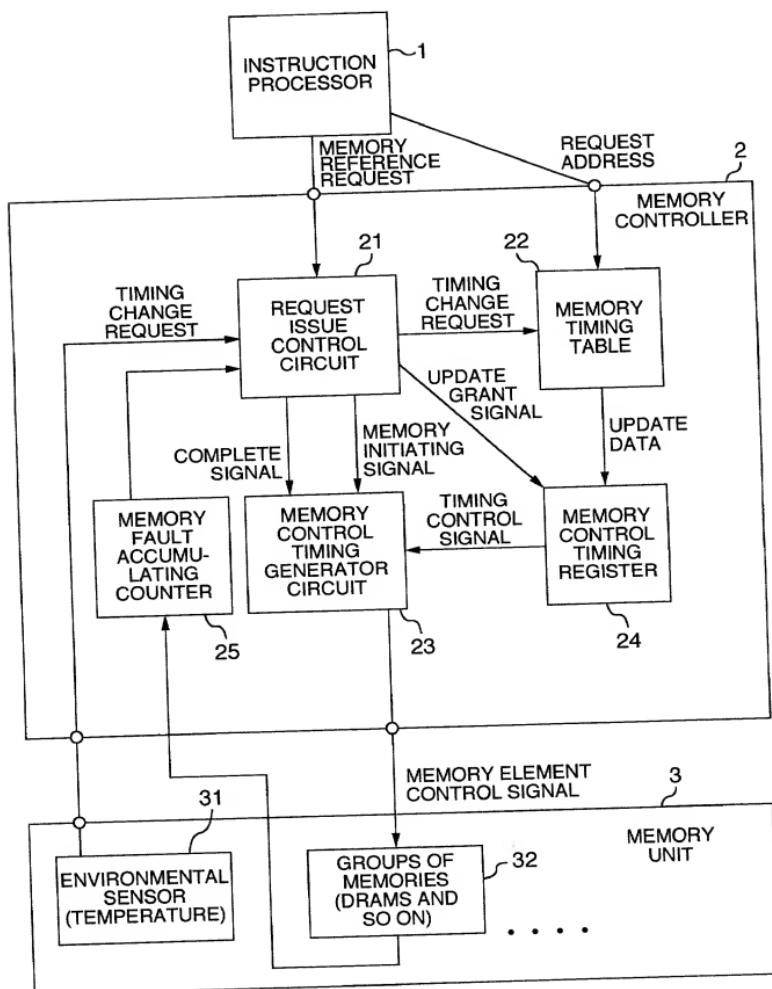


FIG. 2

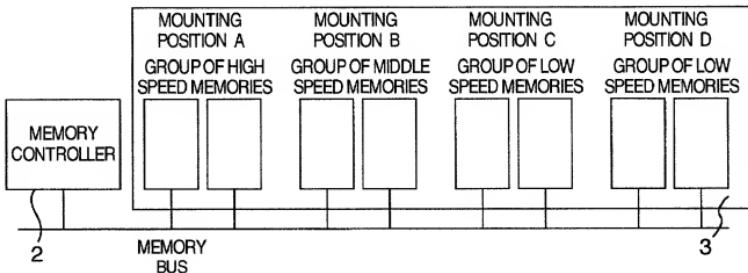


FIG. 3

MOUNTING POSITION	MEMORY TIMING PARAMETERS			
	CLK	RCD	CL	FT
A	10ns	20ns	20ns	10ns
B	10ns	20ns	30ns	10ns
C	15ns	30ns	30ns	10ns
D	15ns	30ns	45ns	15ns

CONTENTS OF MEMORY
TIMING TABLE

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FIG. 4A

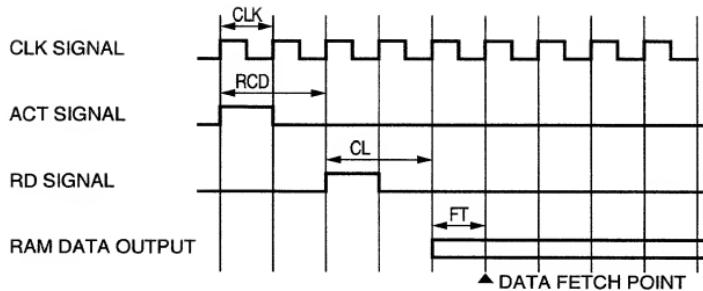


FIG. 4B

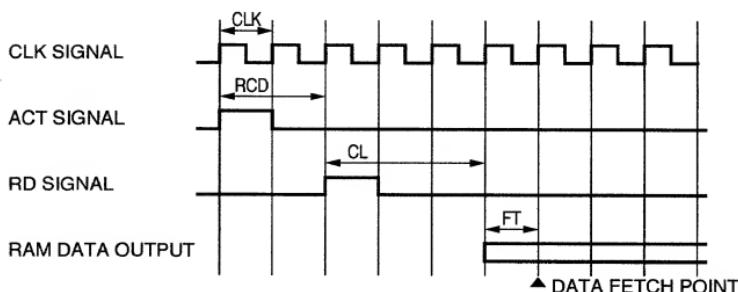
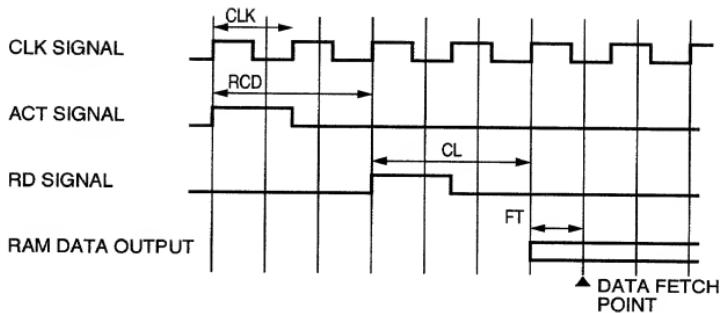
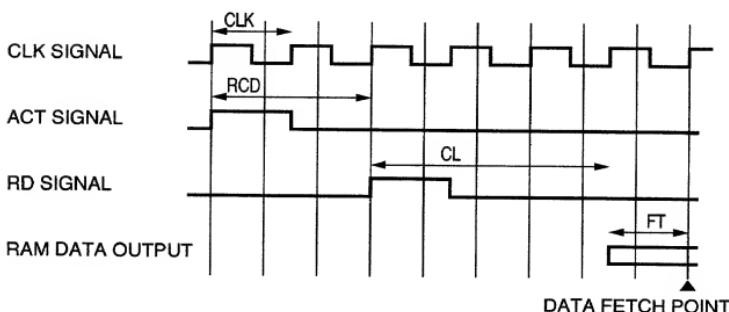


FIG. 5A



SDRAM OPERATION TIMING AT MOUNTING POSITION C

FIG. 5B



SDRAM OPERATION TIMING AT MOUNTING POSITION D